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13. ABSTRACT (Maximum 200 words)

We have investigated a new type of millimeter wave oscillator device based on a resistive gate MESFET structure. The resistive gate establishes a uniform electric field in the regime of negative differential mobility for electrons in GaAs. At these fields, dipolar charge domains form in the channel and drift into the drain, producing microwave oscillations in the drain current. In the contiguous domain mode, a continuous sequence of charge domains forms throughout the channel. This mode is possible because the resistive gate screens the self-induced fields of each dipolar domain, keeping the field outside the domain unperturbed. Frequencies up to 100+ GHz are predicted, independent of channel length, and the frequency should be tunable over at least one octave by varying the gate-to-source voltage. This mode has not yet been observed experimentally, since the gate resistivity on our prototype devices has been too large. These devices are presently operating in a single domain transit time mode, producing oscillations in the 6 to 28 GHz range for channel lengths from 5 to 20 μm. Work is continuing to reduce the gate resistivity so that the contiguous domain mode can be observed.

14. SUBJECT TERMS: CDO, contiguous domain oscillator, RG-MESFET

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Investigation of a New Concept in Semiconductor Microwave Oscillators

Final Report

30 June 1990

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Introduction and Background

In this program we have investigated a new class of monolithic millimeter wave oscillators. These devices are based on the geometry of a resistive gate metal-semiconductor field effect transistor (RG-MESFET). RG-MESFET oscillator devices are attractive because they are easily fabricated on standard MESFET processing lines and can be easily incorporated into planar monolithic millimeter wave integrated circuits (MMICs).

We initially set out to demonstrate that RG-MESFET devices could be used to form a contiguous sequence of Gunn-like charge domains in the channel, the "contiguous domain mode". Such devices are referred to as contiguous domain oscillators, or "CDOs". In the process of this research, we learned that several design conditions must be met in order that contiguous domains can form, and if these conditions are not met, then other oscillation modes are observed instead. The most interesting of these "other" modes is the single-domain transit time mode. It is also possible to fabricate RG-MESFET devices with channel doping too low to allow charge domains to form at all. These devices exhibit a strong stable negative transconductance which might also be used as the basis for a microwave oscillator.

The contiguous domain oscillator (CDO) is an RG-MESFET in which a sequence of contiguous dipole domains form spontaneously and continuously in the channel near the source and propagate along the channel into the drain. This unique behavior was first predicted by computer simulations, and arises because of the two dimensional nature of the electrostatic boundary conditions in the device. Simulations indicate that the frequency of oscillation is not related to the channel length, but instead is determined by the domain width and the drift velocity. The domain width (or spatial period) is inversely proportional to the average electron density in the channel, a quantity which is controlled by the gate-to-source voltage. Thus it is possible to modulate the frequency during operation by varying the gate-to-source voltage. Frequencies in the range from a few GHz to over 100 GHz are predicted, independent of channel length.

In this report we will outline the accomplishments of approximately five years of sponsored research, the first three years under grant no. AFOSR-85-0193 and the last two years under a continuation grant and no-cost extensions.

Research Objectives

The major objective of this research was to fabricate and characterize resistive gate MESFET oscillators. It was hoped that the contiguous domain mode would be observed. As will be seen, the CDO mode has not yet been realized, but RG-MESFET devices have been operated in the single-domain transit time mode, producing microwave oscillations in the range from 6 to 28 GHz.

Status of the Research

A. Fabrication of Experimental Devices

Experimental devices in the form of resistive gate MESFETs were designed at Purdue, and masks were sent to the ITT Gallium Arsenide Technology Center in Roanoke, VA, for fabrication. A cross section of the experimental device is shown in Fig 1. Six wafers containing several thousand devices each were started in late 1987, and three of the original six were delivered to Purdue on 23 February, 1988. The wafers had been fabricated with a range of channel depths and dopings in an attempt to bracket the optimum design. A summary of the six wafers is given below, where the asterisk indicates those wafers which actually completed the process and were received at Purdue.

Wafer No.	Channel Depth	Channel Doping
CDO-1-1	2000 Å	$1x10^{17}$ cm^{-3}
CDO-1-2	2000 Å	$2x10^{17}$ cm^{-3}
CDO-1-3*	2000 Å	$4x10^{17}$ cm^{-3}
CDO-1-4*	1500 Å	$5x10^{16}$ cm^{-3}
CDO-1-5*	1500 Å	$1x10^{17}$ cm^{-3}
CDO-1-6	1500 Å	$2x10^{17}$ cm^{-3}

Of the three wafers received at Purdue, CDO-1-3 showed essentially no modulation of drain current under wide variations in gate bias, probably due to the high doping level and thick channel. Wafer CDO-1-5 had substantial modulation, but it's characteristics seemed less ideal than those of CDO-1-4. Examples of I-V curves with the oscillator devices operated as simple MESFETs (V_{GG}=0) are shown in Fig. 2.

Wafer CDO-1-4 was chosen for the initial measurements. It was soon found that any attempt to operate these devices with a non-zero lateral gate field (i.e. V_{GG}>0) resulted in early device failure. This failure was caused by a design decision to place the ohmic contact to the resistive gate 5 µm back from the edges of the source and drain regions, as shown in Fig. 3. At the lateral gate fields necessary for domain formation to occur ($E \approx 1$ V/µm) the potential of the gate at a point directly over the edge of the drain was about 5 V more negative than the potential at the ohmic contact. Since the gate-to-drain breakdown voltage was only about 4 V, the devices failed due to gate-drain breakdown.

The design oversight was corrected on a portion of wafer CDO-1-4 by reprocessing at Purdue. This consisted of plasma etching the SiN cap layer and evaporating a layer of aluminum to extend each ohmic contact closer to the edges of the source and drain, as illustrated in Fig. 4. The lithography for these operations was done by direct write on wafer using our Cambridge EBMF electron beam lithography system. Once the modifications had been made, the devices on CDO-1-4 no longer failed upon application of the gate field, and DC bias could be maintained indefinitely at the level necessary for microwave testing.

B. Microwave Testing of Wafer CDO-1-4

The section of wafer CDO-1-4 which had been modified to have the extended ohmic contacts was sawed into individual chips, each containing eighteen CDO devices. The test chips were mounted on a TO-5 package and one CDO device was wire bonded to the pins of the package, as shown in the upper portion of Fig. 5. The TO-5 package was mounted in a waveguide insertion unit as shown in the lower portion of Fig. 5. The insertion unit was WR-28 size, having operating frequency range of 26-40 GHz. It was not possible to mount the CDO test chip into a smaller cavity owing to the dimensions of the test chip, about 2.4 mm per side. The waveguide insertion unit was terminated at one end by a sliding short, and the other end connected through a slide screw tuner to a Tektronix waveguide mixer. Mixers covering the bands 26-40, 40-60, and 60-90 GHz were used sequentially. The mixer was connected to a Tektronix 2755 spectrum analyzer capable of tuning to 325 GHz. Tests were run with a resolution bandwidth of 1 MHz with a sensitivity of around -50 to -70 dBm.

Several devices were tested using the arrangement of Fig. 5. During testing, the biases to the CDO device were systematically varied, as was the position of the sliding short and the slide-screw tuner. The frequency range from 26 to 90 GHz was covered with no evidence of oscillation. Subsequent calculations indicated that the devices on wafer CDO-1-4 had a channel doping -- channel thickness squared ($N_D\, t_{epi}^2$) product which is too low for domain formation to occur.

Wafer CDO-1-5 had a channel doping of $1.2\text{x}10^{17}$ cm^{-3}, twice as large as wafer CDO-1-4. Repeating the calculation for the devices on wafer CDO-1-5 indicated the $N_D\, t_{epi}^2$ product was large enough to allow domains to form. For this reason, all subsequent investigations were preformed on devices from wafer CDO-1-5.

C. Microwave Testing of Wafer CDO-1-5

Devices from wafer CDO-1-5 were reprocessed at Purdue to reduce the spacing between the gate contacts and source/drain edges. These devices were again mounted on TO-5 packages, and initial microwave measurements were conducted in the WR-28 waveguide apparatus of Fig. 5. Microwave signals were observed immediately upon application of bias to the first device. The signals were in the range from 37 to 42 GHz, and the frequency could be modulated by gate-to-source bias, as shown in Fig. 6. The operation was highly consistent and repeatable from day to day. Devices could be operated continuously for hours at a time, day after day, with no change in behavior observed.

A number of devices having different width and length were measured, and a summary of their oscillation frequencies is given in Fig. 7. Notice that the frequencies in Fig. 7 are in the range from 22 to 30 GHz, considerably lower than the signals in Fig. 6. After further investigation it became apparent that *each* device produced signals in *both* the 22-30 GHz and 37-42 GHz bands simultaneously, and that these signals always appeared in the ratio 3:2, suggesting that both were harmonics of a fundamental signal in the range of 11 to 15 GHz. This fundamental signal could not be observed directly, since the cutoff frequency of the WR-28 waveguide was 21 GHz. In order to verify the existence of a fundamental signal below 21 GHz, it was necessary to mount the devices on a stripline, as shown in Fig. 8. At this point, we began a careful series of experiments to measure the oscillation frequency and all four terminal currents (I_S, I_D, I_{G1}, and I_{G2}) as a function of each of the three terminal voltages (V_{SG}, V_{GG}, and V_{DG}). The results of these measurements are shown in Figs. 9-11.

Figure 9 shows how frequency and terminal currents depend upon source-to-gate voltage. Note that the frequency ranges from 12.7 to 14.7 GHz as V_{SG} is varied from 5.0 to 6.1 V. Oscillations are not observed for V_{SG} below 4.5 V or above 6 V. The dramatic decrease of source current and increase of gate-1 current for V_{SG} greater than 7 V is due to avalanche breakdown of the gate-to-source junction.

Figure 10 shows that both frequency and current are essentially independent of drain voltage for V_{DG} less than about 4.5 V. This is evidence that conditions in the channel are effectively isolated from the drain due to the screening effect of the resistive gate. For V_{DG} greater than about 4.5 V, the drain current increases rapidly and the gate-2 current decreases, indicating avalanche breakdown of the gate-to-drain junction.

Figure 11 shows frequency and power as a function of gate-to-gate voltage. The output power of a 10 μm wide device ranges between 0.1 and 1 μW for frequencies around 13 GHz. Both the frequencies and the power are much lower than expected for the contiguous domain mode. A considerable amount of effort was expended to make sure no oversights in the theoretical description of the device were responsible for the discrepancy. Eventually, the persistent disagreement with theoretical predictions and the fact that the observed frequencies were essentially equal to the inverse of the transit time from source to drain led us to suspect that these devices were actually operating in a single *domain transit time mode*. This was confirmed by measuring frequencies on devices of different channel length, as shown in Fig. 12.

D. Discussion of Results

The failure of the contiguous domain mode to appear in these devices can be traced to the action of the resistive gate in screening the local fields due to charge domains in the channel. In order for screening to occur, i.e. in order for the gate to provide a linearly varying potential (constant field), it is necessary that local motion of image charges on the gate not appreciably disturb the applied DC electric field. This requires that the gate resistivity be below a critical value. If we require that the local voltage drops on the gate be small compared to the applied field, we can derive a restriction on the gate resistivity ρ_g,

$$\rho_g \, \Delta Q_{RMS} \, v_d << E_A$$

where ρ_g is the sheet resistance of the gate, ΔQ_{RMS} the RMS variation of charge density in the domain, v_d the domain drift velocity, and E_A the applied electrical field. Taking typical values, $E_A = 8000$ V/cm, $\Delta Q_{RMS} = 7\times10^{-8}$ C/cm^2, and $v_d = 1.3\times10^7$ cm/s, then ρ_g should be much less than 9 kΩ per square. The experimental devices on wafer CDO-1-5 has a gate sheet resistance of 30 kΩ per square.

The effect of too high a gate resistivity is illustrated dramatically in Fig. 13, where we show a computer simulation of a device operating in the contiguous domain mode. In this calculation, we assume an ideal gate (i.e. a perfectly linear potential distribution) and calculate the motion of charge domains in the channel. We then assume that on the *real* gate, image charges would move at the same rate as the charges in the channel in order to provide the necessary screening. The figure shows the actual potential variation on the gate at 10 ps intervals for a gate resistivity of 30 kΩ per square. Not only does the potential in the middle of the gate vary with time by almost a factor of two, but at any particular time the potential as a function of position has an oscillatory behavior which produces alternating regions of positive and *negative* electric field. This is observed under conditions where a *uniform positive* electric field is expected and required. Clearly, the violent perturbation of gate potential would have dire consequences for the formation and behavior of domains in the channel. To illustrate the role of gate resistivity in this situation, we show in Fig. 14 the gate potential for the same operating conditions if the gate resistivity were reduced to 3 kΩ per square. With this lower gate resistivity, the linear potential along the gate is virtually undisturbed by the motion of image charges.

E. Work Presently Underway

In order to reduce the resistivity of the gates in our experimental devices, we have developed a procedure for electron beam evaporation of mixed powers of Cr and SiO to form a "cermet" resistive film. In this procedure, the original gate is first removed by plasma etching to expose bare GaAs. The masking photoresist is left on the wafer, and approximately 3000 Å of 55% Cr / 45% SiO weight mixture is evaporated. The cermet film is patterned by liftoff, and a second lithography step is performed by direct electron beam exposure to define gate contacts. A Ti/Au layer is then evaporated and patterned by liftoff. Finally, a thermal annealing step is required to produce low contact resistance. This annealing step also reduces the gate resistivity in a manner which is predictable based on the temperature and duration of the anneal. It is necessary to take this reduction into account when depositing the original cermet film.

The development of this process has taken considerable effort, since fairly low resistivity is required with low contact resistance and good repeatability. We are now ready to apply this procedure to modify devices on wafer CDO-1-5. We have found experimentally that the 3 kΩ cermet film can be biased to the required voltage under DC conditions without burn-out due to heating.

F. Summary

At this point in the program, at the end of Air Force funding, we have not yet reached our goal of demonstrating the contiguous domain mode of operation. We have, however, observed oscillations in the single domain transit time mode, with fundamental frequencies ranging from 6 to 28 GHz as channel length is varied from 20 μm to 6 μm. This mode of operation in a resistive gate MESFET is absolutely unique and is clearly distinct from a lateral Gunn diode. The obvious difference is that the driving field is derived from the resistive gate, and hence the oscillation conditions are independent of and isolated from the drain voltage.

At this point we have every reason to believe that the contiguous domain mode will be obtained in the near future. Clearly, the high value of gate resistance in our present devices would prevent the gate from approximating the ideal linear potential needed for contiguous domain formation. We expect that our efforts to reduce the gate resistance in these devices will be successful, and we hope to observe frequencies in the 60-90 GHz range on the modified devices.

Publications

[1] Y. Yin, J. A. Cooper, Jr., P. G. Neudeck, M. L. Balzan, and A. E. Geissberger, "Negative Transconductance in a Resistive Gate MESFET", submitted to *Appl. Phys. Lett.*, January, 1989.

[2] Y. Yin, J. A. Cooper, Jr., P. G. Neudeck, M. L. Balzan, and A. E. Geissberger, "Room Temperature Negative Transconductance in a Resistive Gate GaAs FET", *WOCSEMMAD*, Hilton Head, SC, February 20-22, 1989.

[3] J. A. Cooper, Jr., Y. Yin, M. L. Balzan, and A. E. Geissberger, "Microwave Characterization of the Contiguous Domain Oscillator," *IEEE Device Research Conference*, Cambridge, MA, June 19-21, 1989.

[4] J. A. Cooper, Jr., Y. Yin, M. L. Balzan, and A. E. Geissberger, "Experimental Verification of the Contiguous Domain Oscillator Concept," *12th IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits*, Ithaca, NY, August 7-9, 1989.

[5] J. A. Cooper, Jr., Y. Yin, M. L. Balzan, and A. E. Geissberger, "Microwave Characterization of a Resistive-Gate MESFET Oscillator," *IEEE Electron Device Lett.* Vol. 10, pp. 493-495, November, 1989.

[6] Y. Yin, H. J. Fu, J. A. Cooper, Jr., M. L. Balzan, and A. E. Geissberger, "Operation of a Resistive Gate MESFET in the Single Domain Transit Time Mode," submitted to *IEEE Electron Device Lett.*

Technical Reports

[1] J. S. Kleine and J. A. Cooper, Jr., "Rapid Thermal Annealing of Silicon Implanted Gallium Arsenide", School of Electrical Engineering, Purdue University, TR-EE 86-43, December, 1986.

[2] Y. Yin, J. A. Cooper, Jr., and H. Fu, "Investigation of a Resistive-Gate MESFET Contiguous Domain Oscillator", School of Electrical Engineering, Purdue University, TR-EE 90-25, April, 1990.

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Ming Fang, MS 1985
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John S. Kleine, MS 1986
Thesis title: "Rapid Thermal Annealing of Silicon Implanted Gallium Arsenide"

Robert E. Beaty, Ph.D 1988
Thesis title: "A Bias Tunable Monolithic Microwave Oscillator -- The Contiguous Domain Oscillator"

Yiwen Yin, Ph.D 1990.
Thesis title: "Investigation of the MESFET Version Contiguous Domain Oscillator"

Hua Julia Fu, Ph.D in progress

Industrial Interactions

We have received substantial support from the ITT Gallium Arsenide Technology Center, Roanoke, VA, in the form of device fabrication and consulting on microwave testing. Industrial interest has also been expressed by the Magnavox government systems division in Ft. Wayne, IN, and by the Magnavox GaAs group in Torrance, CA.

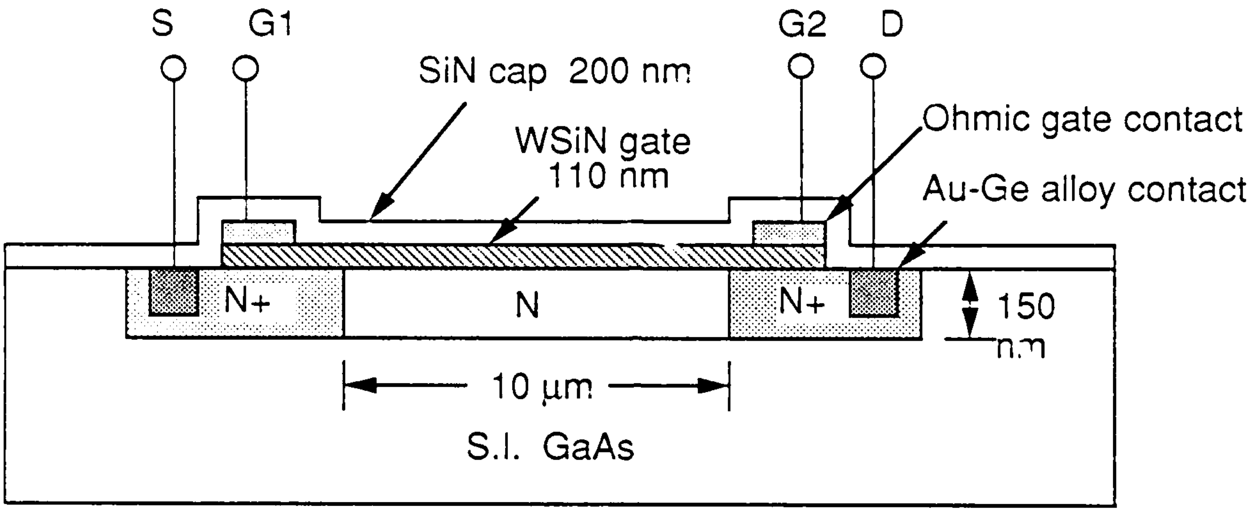
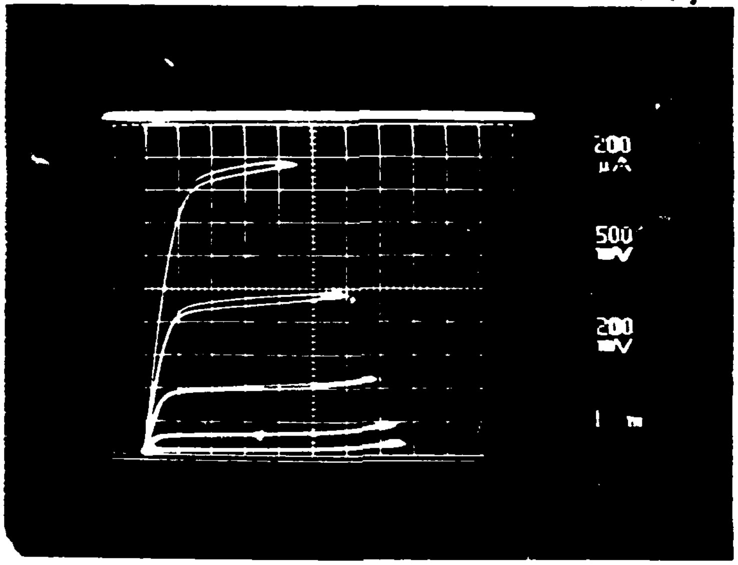
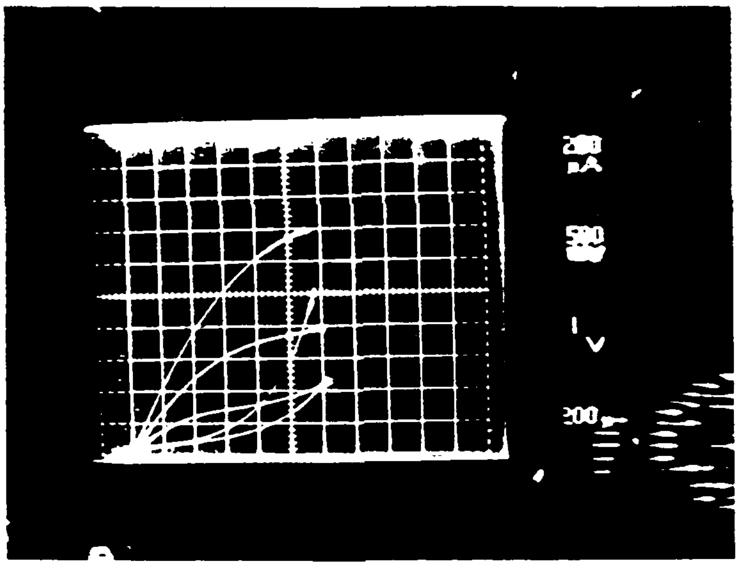


Figure 1. Cross section of RG-MESFET devices fabricated by ITT Gallium Arsenide Technology Center.



I-V before Test zero mid

3/6/88 CDO 1-5 20x20 B



I-V curve as Transistor. zero mid.

Figure 2. Curve tracer photos of RG-MESFET devices from wafer CDO-1-4 (top) and CDO-1-5 (bottom) operated as MESFETs (i.e. with G1 connected to G2).

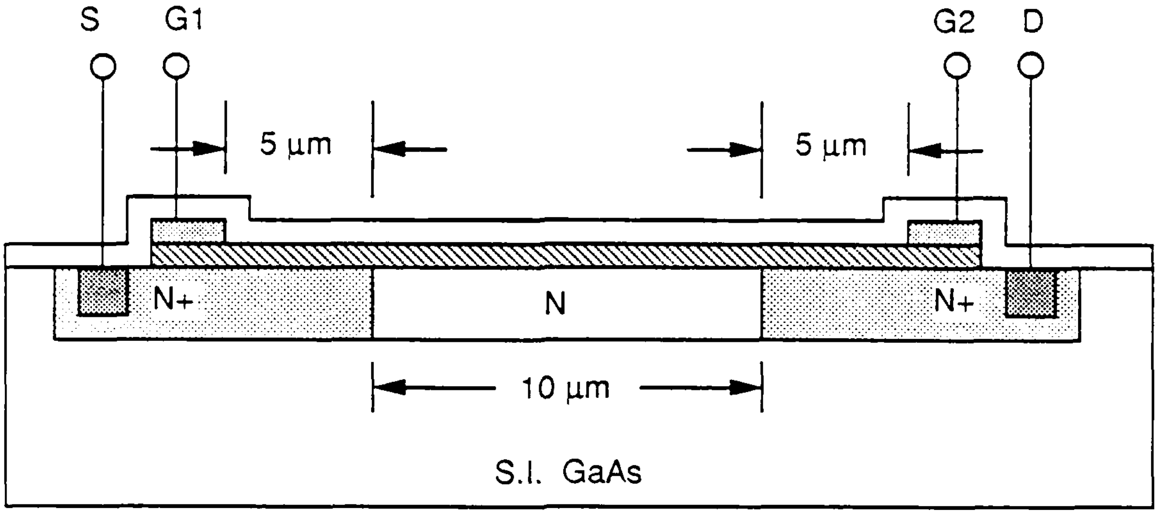


Figure 3: Cross section of RG-MESFET devices showing typical dimensions. The 5 µm separation between gate contact the the edge of the source/drain junctions lead to undesirable voltage drop along the portion of the resistive gate over the source and drain.

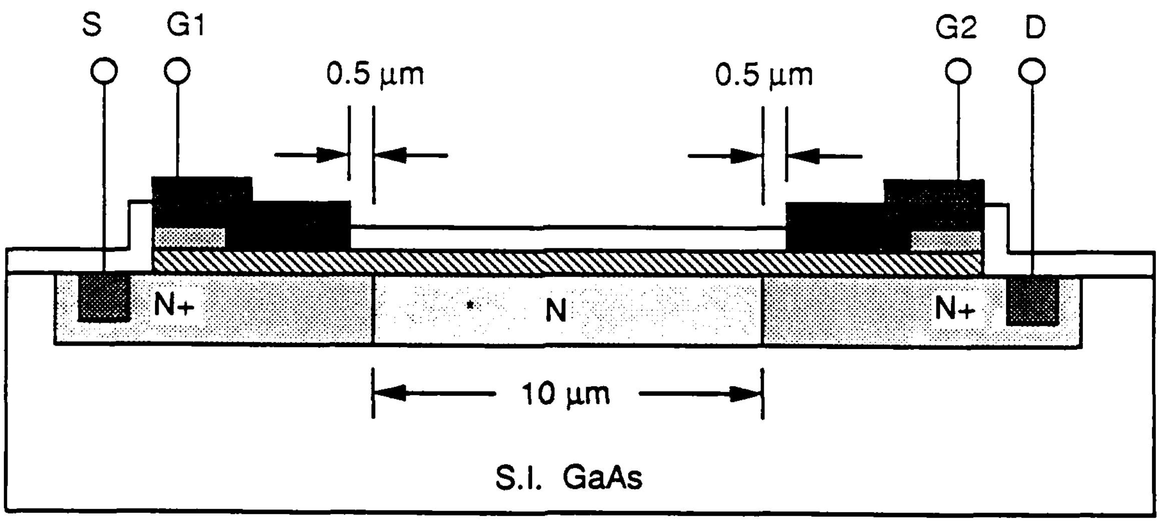


Figure 4. Cross section of the experimental CDO device after the gate ohmic contacts had been modified at Purdue. The structure shown above can sustain continuous DC biasing at fields high enough to allow domain formation.

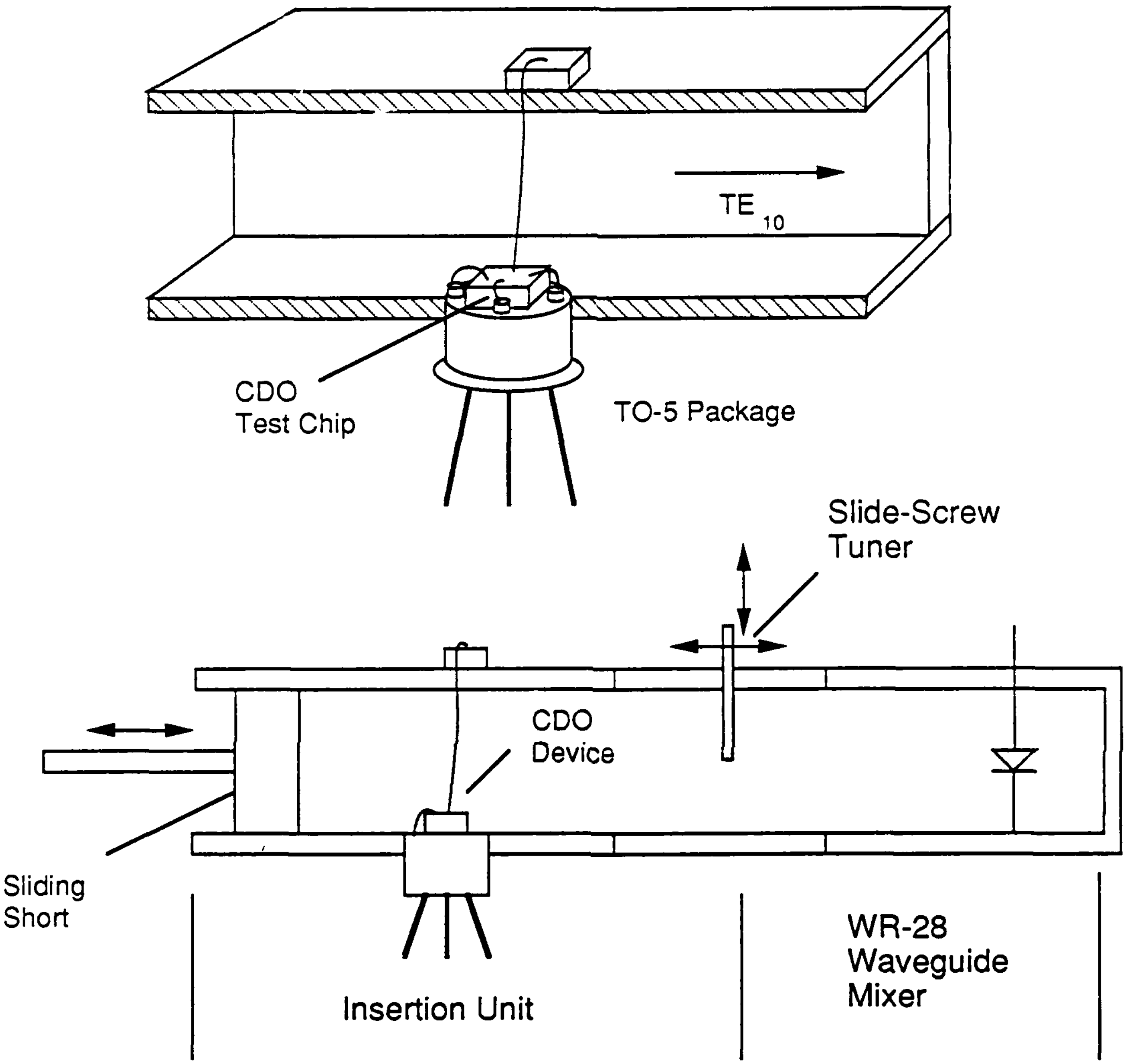


Figure 5. Top View: Cross section of mounting arrangement with the drain wire of the CDO device connected through a slot in the top of the waveguide, serving as an E-field antenna. Bottom View: Cross section of entire waveguide apparatus, including sliding short and slide-screw tuner.

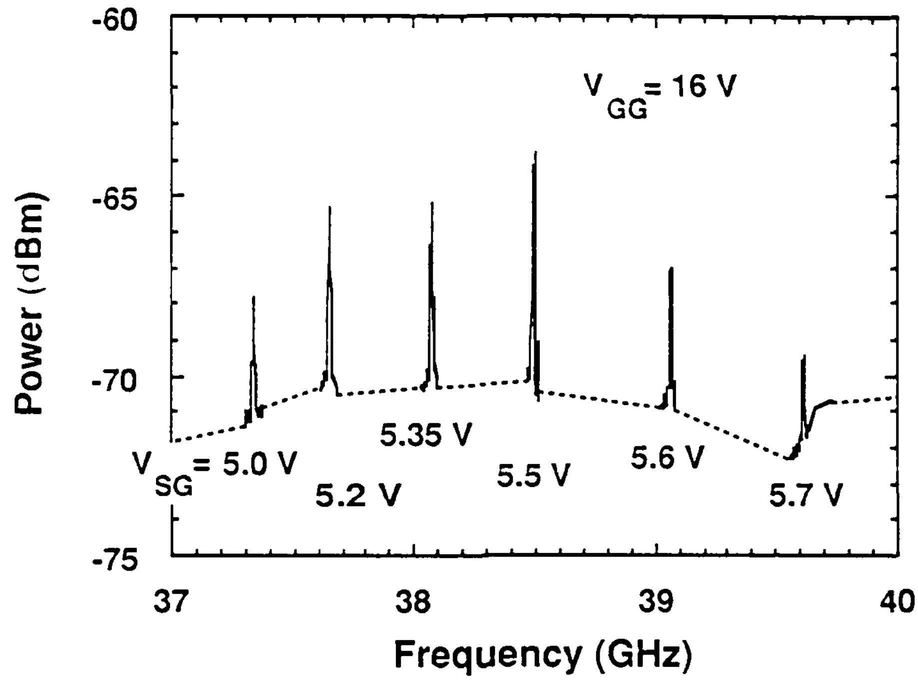


Figure 6. Power spectra for the first observed microwave oscillation from wafer CDO-1-5. The figure shows a series of spectra obtained at different values of source-to-gate bias.

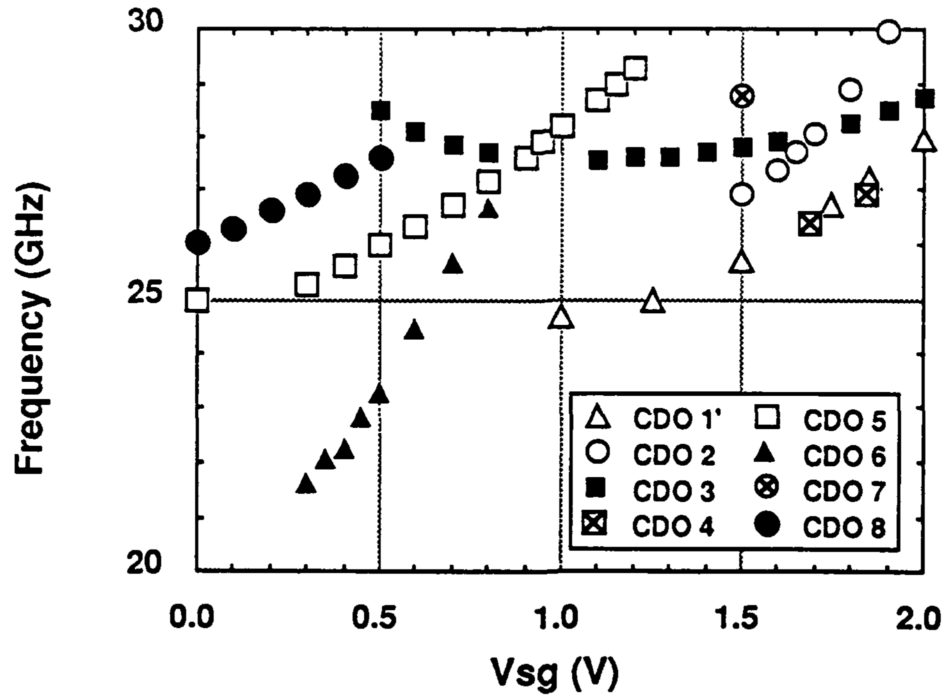


Figure 7. Oscillation frequency of several CDO devices from wafer CDO-1-5 as a function of source-to-gate voltage. The gate field is 8000 V/cm. Channel width and length are: CDO 1', 2, and 3 (10x10 µm), CDO 4 (10x20 µm), CDO 5 (20x10 µm), CDO 6 (20x20 µm), CDO 7 (10x50 µm), CDO 8 (200x10 µm).

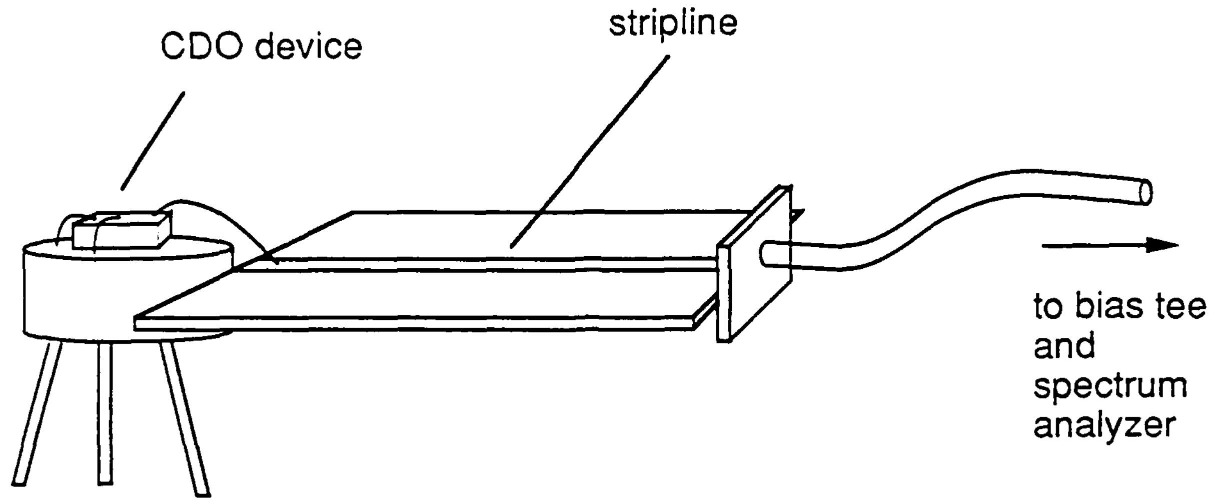


Figure 8: Stripline mounting arrangement for CDO testing. Bias is supplied via pins on the TO-5 can, while the microwave signal is taken out via the stripline to the spectrum analyzer. A bias tee is inserted between the stripline and the spectrum analyzer (not shown) to bias the drain.

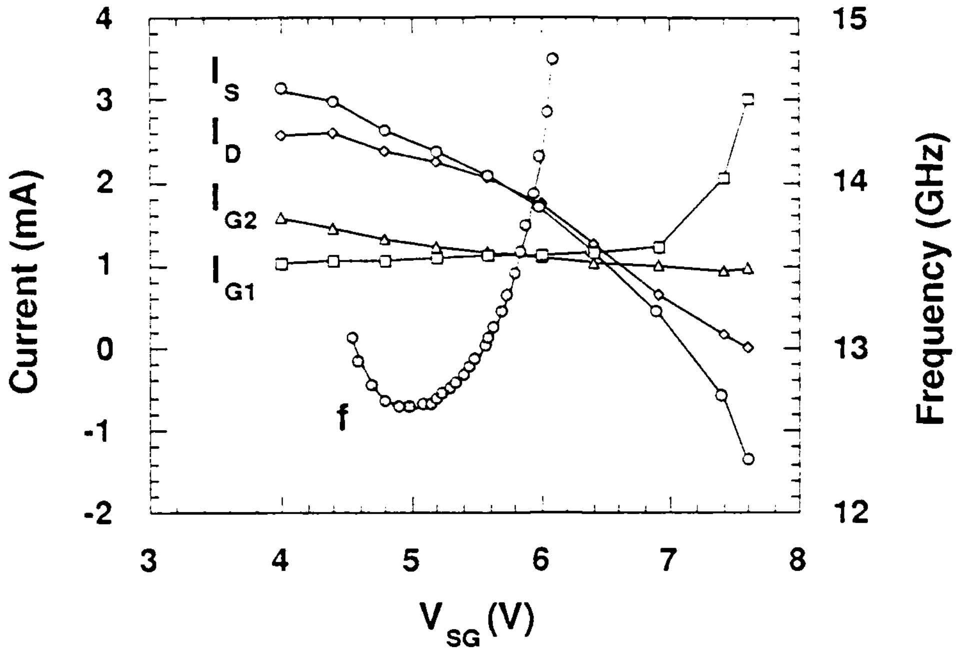


Figure 9. Frequency and terminal currents as a function of source-to-gate voltage with gate field constant at 8000 V/cm. Drain-to-gate voltage is zero.

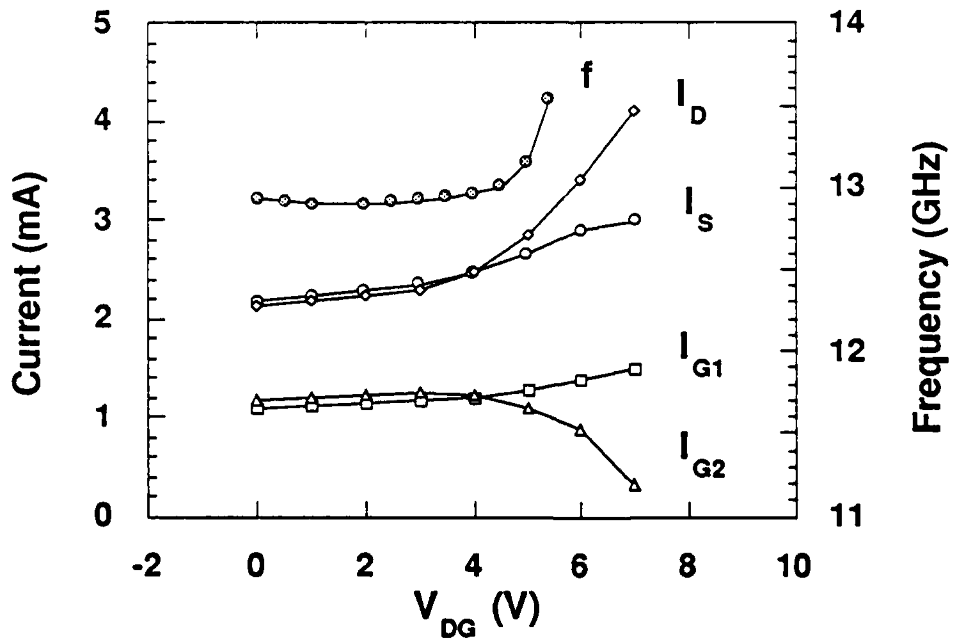


Figure 10. Frequency and terminal currents as a function of drain-to-gate voltage with gate field constant at 8000 V/cm. Source-to-gate voltage is held at 5.5 V.

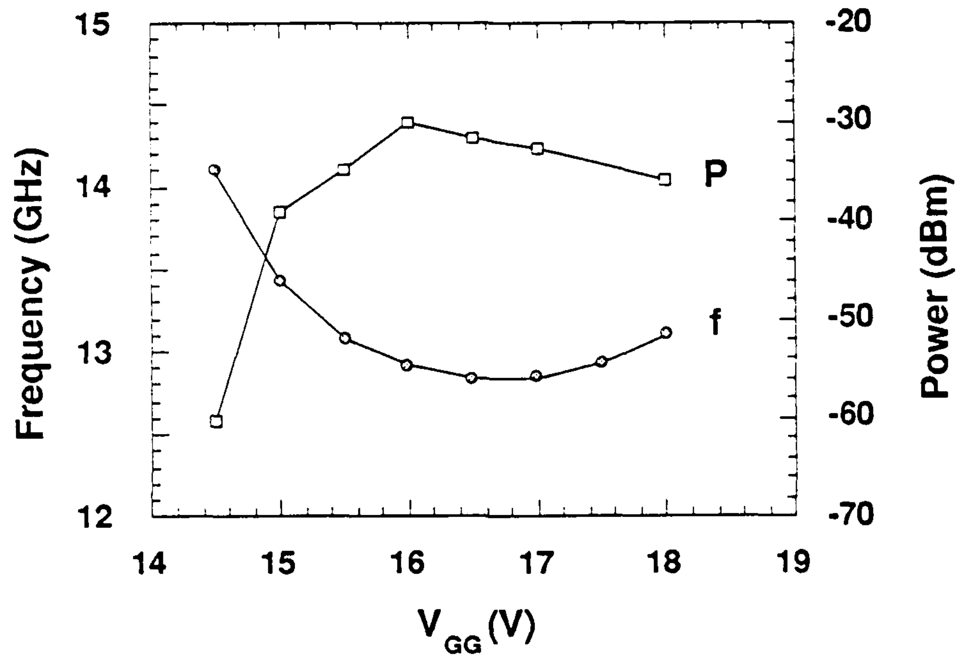


Figure 11. Frequency and microwave power as a function of gate-to-gate voltage. Source-to-gate voltage is 5.5 V and drain-to-gate voltage is zero.

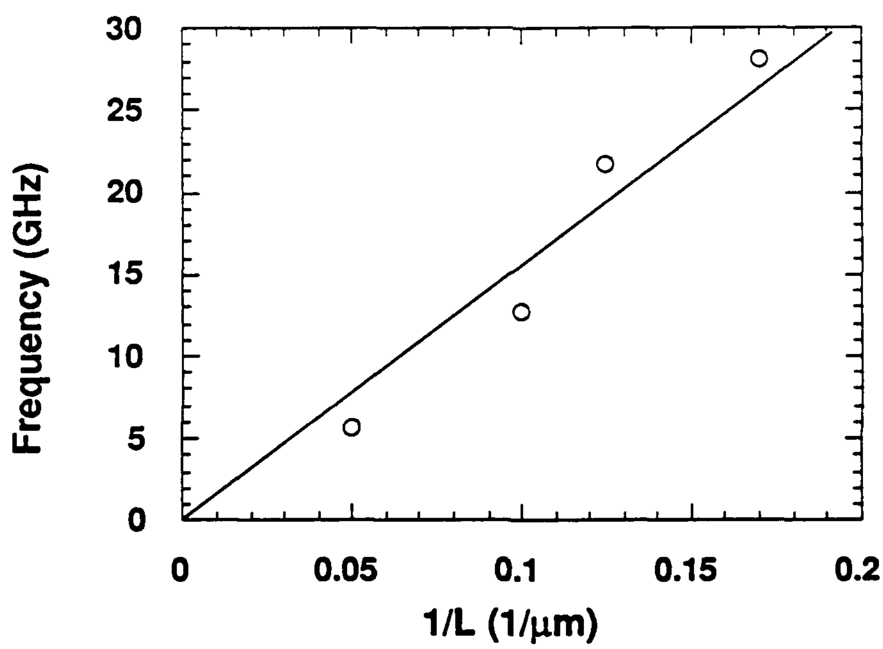


Figure 12. Frequency versus reciprocal channel length for four CDO devices from wafer CDO-1-5. The linear dependence indicates that the devices are operating in the single domain transit time mode.

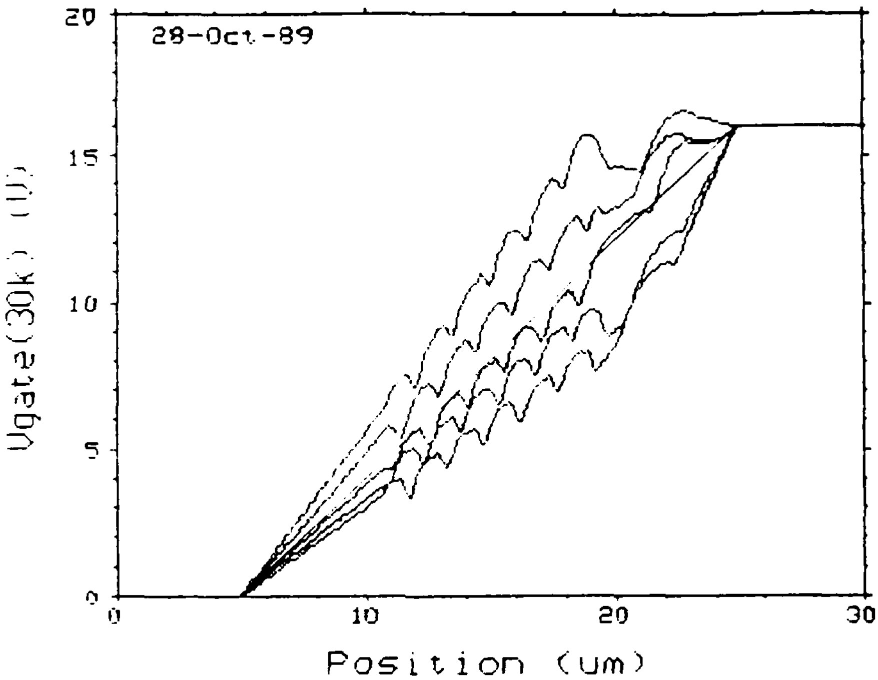


Figure 13. Potential of resistive gate versus position at 10 ps intervals during operation assuming that charges move in the channel as though the gate were ideal. Gate resistivity is 30 kΩ per square. Note that the gate potential is significantly perturbed by the motion of image charges.

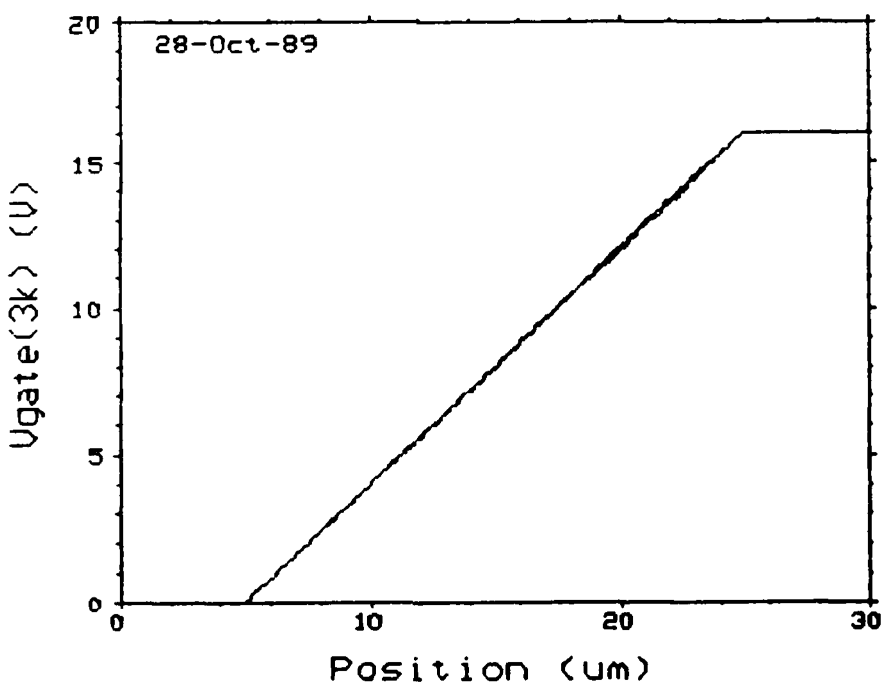


Figure 14. Potential of resistive gate for the same conditions as Fig 13, except that the gate sheet resistance is reduced to 3 kΩ per square. At this value of gate resistivity, the potential is virtually undisturbed by the motion of image charges.